CAP1005 / CAP1006

5 and 6 Channel Capacitive Touch Sensor

PRODUCT FEATURES

Datasheet

General Description

The CAP1006 and CAP1005 are multiple channel Capacitive Touch sensors. The CAP1006 contains six (6) individual Capacitive Touch sensor inputs while the CAP1005 contains five (5) sensors. Both devices offer programmable sensitivity for use in touch sensor applications. Each sensor automatically recalibrates to compensate for gradual environmental changes.

The CAP1005 / CAP1006 offers multiple power states operating at low quiescent currents.

During the Standby mode of operation, one or more Capacitive Touch Sensors are active.

The Deep Sleep mode of operation is the lowest power state available drawing 3uA of current. During this mode, no sensors are active. Communications will wake the device.

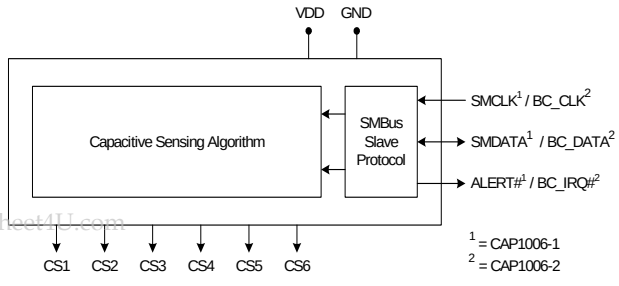
Applications

- Desktop and Notebook PC's
- LCD Monitors
- Printers
- Appliances

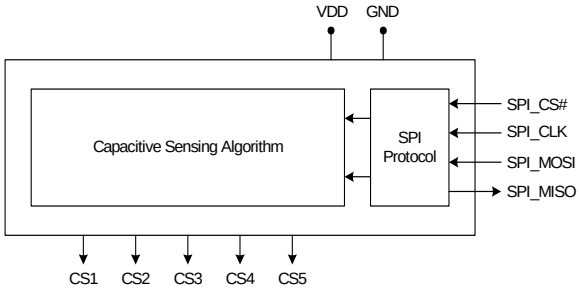
Features

- Six (6) Capacitive Touch Sensor Inputs - CAP1006
- Five (5) Capacitive Touch Sensor Inputs - CAP1005
  - Programmable sensitivity
  - Automatic recalibration
  - Individual thresholds for each button
- Flexible Capacitive Touch Sense algorithm
- Multiple Communication interfaces
  - SMBus / I^{2}C compliant interface (CAP1006-1 only)
  - SMSC BC-Link interface (CAP1006-2 only)
  - SPI communications (CAP1005 only)
- Low Power operation
  - 3uA quiescent current in Deep Sleep
  - Samples one or more channels in Standby
  - Open Drain or Push-Pull
- Available in 10-pin 3mm x 3mm RoHS compliant DFN package

CAP1006 Block Diagram



CAP1005 Block Diagram



Note: I^{2}C is a trademark of NXP semiconductor. BC-Link is a trademark of SMSC.

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	FEATURES
CAP1006-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead Free RoHS compliant)	Six Capacitive Touch Sensors, SMBus interface
CAP1006-2-AIA-TR	10-pin DFN 3mm x 3mm (Lead Free RoHS compliant)	Six Capacitive Touch Sensors, BC-Link interface
CAP1005-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead Free RoHS compliant)	Five Capacitve Touch sensors, Full Duplex SPI interface

REEL SIZE IS 4,000 PIECES

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 Pin Description

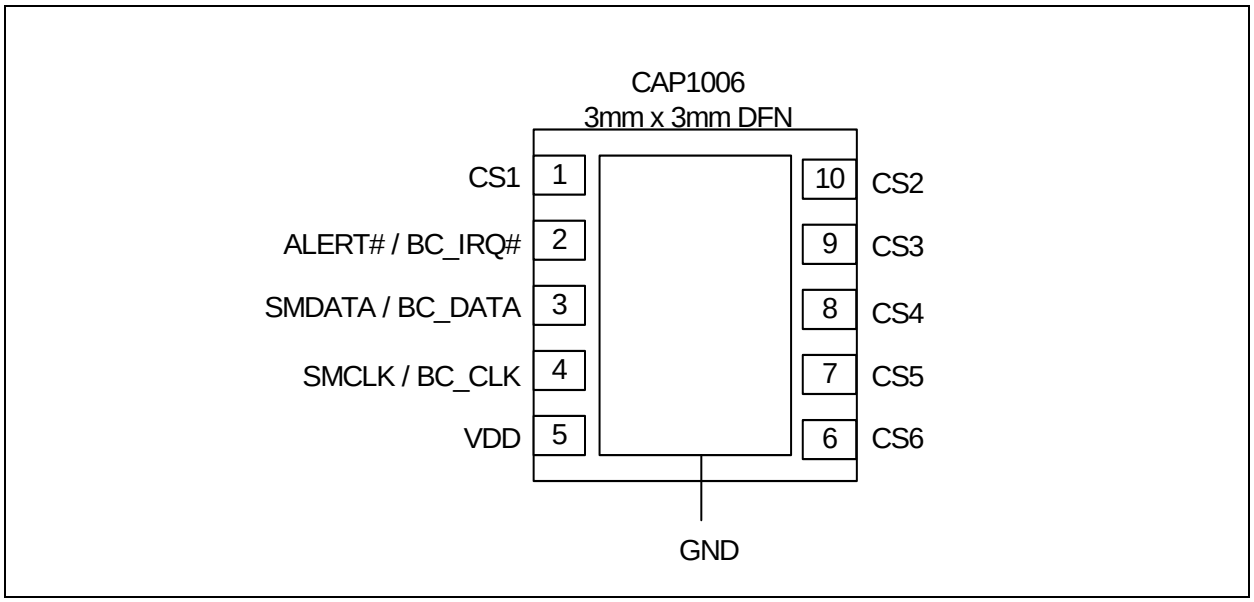


Figure 1.1 CAP1006 Pin

Table 1.1 Pin Description for CAP1006

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	CS1	Capacitive Touch Sensor 1	AIO
2	ALERT# / BC_IRQ#	ALERT# - Active low alert / interrupt output usable for SMBus alert (CAP1006-1)	OD (5V)
		BC_IRQ# - Active low interrupt / optional for BC-Link (CAP1006-2)	OD (5V)
3	SMDATA / BC_DATA	SMDATA - Bi-directional, open-drain SMBus data - requires pull-up resistor (CAP1006-1)	DIOD (5V)
		BC_DATA - Bi-directional, open-drain BC-Link data - requires pull-up resistor (CAP1006-2)	DIO
4	SMCLK / BC_CLK	SMCLK - SMBus clock input - requires pull-up resistor (CAP1006-1)	DI (5V)
		BC_CLK - BC-Link clock input (CAP1006-2)	DI (5V)
5	VDD	Positive Power supply	Power
6	CS6	Capacitive Touch Sensor 6	AIO
7	CS5	Capacitive Touch Sensor 5	AIO
8	CS4	Capacitive Touch Sensor 4	AIO
9	CS3	Capacitive Touch Sensor 3	AIO

Table 1.1 Pin Description for CAP1006 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
10	CS2	Capacitive Touch Sensor 2	AIO
Bottom Pad	GND	Ground	Power

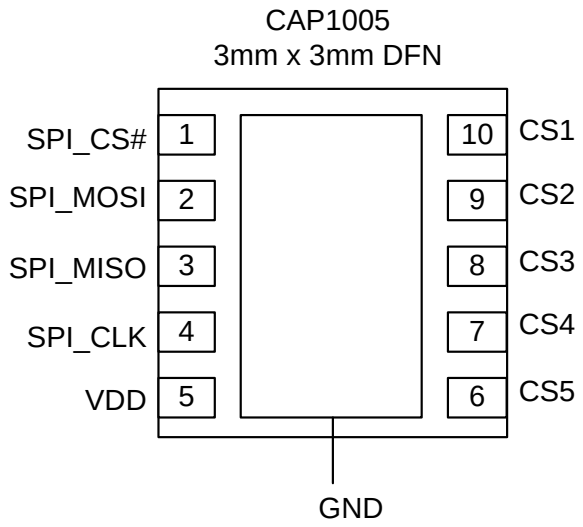


Figure 1.2 CAP1005 Pin Diagram

Table 1.2 Pin Description for CAP1005

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	SPI_CS#	Active low chip-select for SPI bus	DI (5V)
2	SPI_MOSI	SPI_MOSI - SPI Master-Out-Slave-In port	DI (5V)
3	SPI_MISO	SPI Master-In-Slave-Out data port	DO
4	SPI_CLK	SPI clock input	DI (5V)
5	VDD	Positive Power supply	Power
6	CS5	Capacitive Touch Sensor 5	AIO
7	CS4	Capacitive Touch Sensor 4	AIO
8	CS3	Capacitive Touch Sensor 3	AIO
9	CS2	Capacitive Touch Sensor 2	AIO

Table 1.2 Pin Description for CAP1005 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
10	CS1	Capacitive Touch Sensor 1	AIO
Bottom Pad	GND	Ground	Power

The pin types are described in detail below. All pins labeled with (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the CAP1005 / CAP1006 is unpowered.

Table 1.3 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - This pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output -This pin is used as an I/O for analog signals.
DIOD	Digital Input / Open Drain Output- This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DO	Push-pull Digital Output - This pin is used as a digital output and can sink and source current.
DIO	Push-pull Digital Input / Output - This pin is used as an I/O for digital signals.

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{5VT_PIN})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_PIN} - V_{DD}\|$) Note 2.2	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation up to T_A = 85°C for 10 pin DFN (see Note 2.3)	0.7	W
Junction to Ambient (θ_{JA})	77.7	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	8000	V

Note 2.1 Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.2 For the 5V tolerant pins that have a pull-up resistor, the voltage difference between V_{5VT_PIN} and V_{DD} must never exceed 3.6V.

Note 2.3 The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 2x2 matrix of 0.3mm (12mil) vias at 1.0mm pitch connected to the ground plane with a 1.6 x 2.3mm thermal landing.

Table 2.2 Electrical Specifications

V_{DD} = 3V to 3.6V, T_A = 0°C to 100°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{STBY}		160	210	uA	Standby state active 1 sensor monitored Default conditions (8 avg, 70ms cycle time)
	I_{DSLEEP}		3	10	uA	Deep Sleep state active No communications T_A < 85°C
	I_{DD}		300	500	uA	Average current Capacitive Sensing Active
Capacitive Touch Sensor						

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 100°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Maximum Base Capacitance	C_{BASE}		50		pF	Pad untouched
Detectable Capacitive Shift	ΔC_{TOUCH}	0.1		2	pF	Pad touched
I/O Pins - SPI_CS#, SPI_MOSI, and ALERT# pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 4mA
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C
SMDATA / BC_DATA / SPI_MSIO / SPI_MISO and SMCLK / BC_CLK / SPI_CLK pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8mA
Output High Voltage	V_{OH}	V_{DD} - 0.4			V	I_{SOURCE_IO} = 8mA
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V
SMBus First Communication	t_{SMB}			15	ms	
SMBus Timing (CAP1006-1 only)						
Input Capacitance	C_{IN}		5		pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 100°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Capacitive Load	C_{LOAD}			400	pF	per bus line
BC-Link Timing (CAP1006-2 only)						
Clock Period	t_{CLK}	250			ns	
Data Hold Time	$t_{HD:DAT}$	0			ns	
Data Setup Time	$t_{SU:DAT}$	30			ns	Data must be valid before clock
Clock Duty Cycle	Duty	40	50	60	%	
SPI Timing (CAP1005 only)						
Clock Period	t_P	250			ns	
Clock Low Period	t_{LOW}	0.4 x t_P		0.6 x t_P	ns	
Clock High Period	t_{HIGH}	0.4 x t_P		0.6 x t_P	ns	
Clock Rise / Fall time	t_{RISE} / t_{FALL}			0.1 x t_P	ns	
Data Output Delay	$t_{D:CLK}$			10	ns	
Data Setup Time	$t_{SU:DAT}$	20			ns	
Data Hold Time	$t_{HD:DAT}$	20			ns	
SPI_CS# to SPI_CLK setup time	$t_{SU:CS}$	0			ns	
Wake Time	t_{WAKE}	10		20	us	SPI_CS# asserted to CLK assert

Chapter 3 Communications

3.1 Communications

The CAP1006-1 communicates using the SMBus or I^2C protocol. The CAP1006-2 communicates using the 2-wire proprietary BC-Link protocol. The CAP1005 communicates using 4-wire SPI bus. Regardless of the communications mechanism, the device functionality remains unchanged.

3.1.1 SMBus (I^2C) Communications

When configured to communicate via the SMBus, the CAP1006 supports the following protocols: Send Byte, Receive Byte, Read Byte, and Write Byte. In addition, the device supports I^2C formatting for block read and block write protocols.

See Section 3.2 and Section 3.3 for more information on the SMBus bus and protocols respectively.

3.1.2 SPI Communications

The CAP1005 is configured to communicate via SPI bus, using a 4-wire protocol. It does not support the 3-wire protocol.

See Section 3.4 and Section 3.5 for more information on the SPI bus and protocols respectively.

3.1.3 BC-Link Communications

When BC-Link communications are used, the CAP1006 supports the read byte protocol and the write byte protocol.

See Section 3.6 for more information on the BC-Link Bus and protocols respectively.

APPLICATION NOTE: Upon power up, the CAP1006 will not respond to any communications for up to 15ms. After this time, full functionality is available.

3.2 System Management Bus

The CAP1006 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the CAP1006 will not stretch the clock signal.

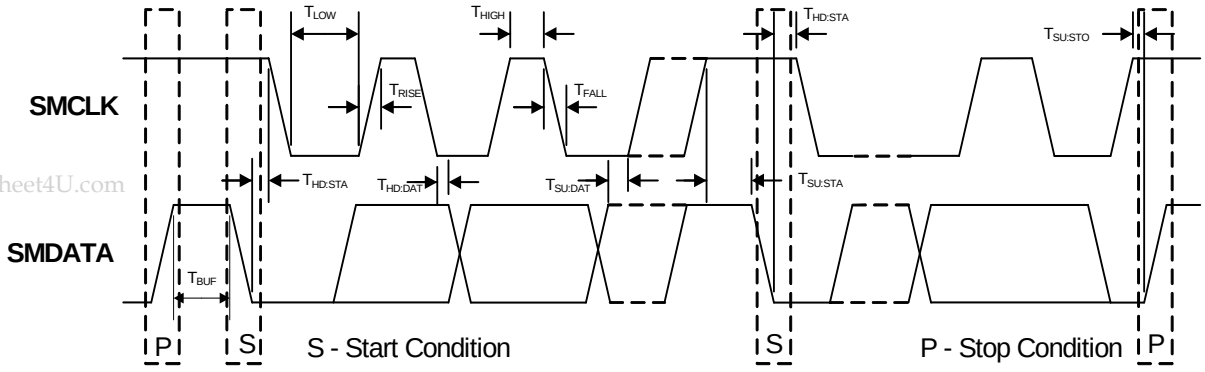


Figure 3.1 SMBus Timing Diagram

3.2.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

3.2.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The CAP1006-1 responds to SMBus address 0101_000(r/w).

3.2.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.2.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

3.2.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the CAP1006 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.2.6 SMBus Timeout

The CAP1006 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will timeout and reset the SMBus interface.

The timeout function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see Section 5.6).

3.2.7 SMBus and I^2C Compliance

The major difference between SMBus and I^2C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held low longer than 30ms.
3. The client protocol will reset if both the clock and the data line are high for longer than 150us (idle condition).
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).
5. I^2C devices support block read and write differently. I^2C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The CAP1006 supports I^2C formatting only.

3.3 SMBus Protocols

The CAP1006 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Block Read, Receive Byte as valid protocols as shown below. The CAP1006 also supports the I^2C block read and block write protocols. Finally, it will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 3.1.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Data sent	Data sent

3.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 3.2.

Table 3.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 ->0	0101_000	0	0	XXh	0	XXh	0	0 -> 1

3.3.2 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 3.3. It is an extension of the Write Byte Protocol.

APPLICATION NOTE: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.3 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	0101_000	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.3.3 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.4.

Table 3.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	CLIENT ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh	1	0 -> 1

3.3.4 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 3.5. It is an extension of the Read Byte Protocol.

APPLICATION NOTE: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.5 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh
ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	REGISTER DATA	ACK	. . .	REGISTER DATA	NACK	STOP
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.3.5 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.6.

Table 3.6 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	0101_000	0	0	XXh	0	0 -> 1

3.3.6 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.7.

Table 3.7 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	0101_000	1	0	XXh	1	0 -> 1

3.4 SPI Interface (CAP1005 only)

The SMBus has a predefined packet structure, the SPI does not. The SPI Bus can operate in two modes of operation, normal 4-wire mode and bi-directional 3-wire mode. The CAP1005 only supports normal 4-wire mode. All SPI commands consist of 8-bit packets set to a specific slave device (identified by the CS pin).

The SPI bus will latch data on the rising edge of the clock and the clock and data both idle high.

All commands are supported via both operating modes. The supported commands are: Reset Serial interface, set address pointer, write command and read command. Note that all other codes received during the command phase are ignored and have no effect on the operation of the device.

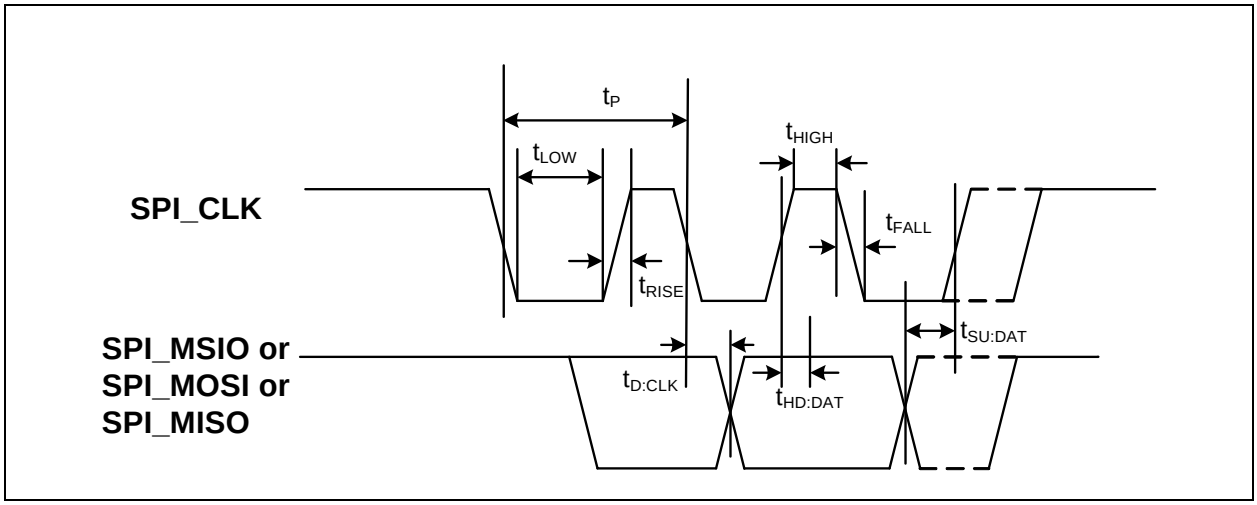


Figure 3.1 SPI Timing

3.4.1 SPI Normal Mode

In the normal mode of operation, there are dedicated input and output data lines. The host communicates by sending a command along the CAP1005 SPI_MOSI data line and reading data on the SPI_MISO data line. Both communications occur simultaneously which allows for larger through put of data transactions.

All basic transfers consist of two 8 bit transactions from the Master device while the slave device is simultaneously sending data at the current address pointer value.

Data writes consist of two or more 8-bit transactions. The host sends a specific write command followed by the data to write the address pointer. Data reads consist of one or more 8-bit transactions. The host sends the specific read data command and continues clocking for as many data bytes as it wishes to receive.

3.4.2 SPI_CS# Pin

The SPI Bus is a single master, multiple slave serial bus. Each slave has a dedicated CS pin (chip select) that the master asserts low to identify that the slave is being addressed. There are no formal addressing options.

3.4.3 Address Pointer

All data writes and reads are accessed from the current address pointer. In both Bi-directional mode and Full Duplex mode, the Address pointer is automatically incremented following every read command or every write command.

The address pointer will return to 00h after reaching FFh.

3.4.4 SPI Timeout

The CAP1005 does not detect any timeout conditions on the SPI bus.

3.5 Normal SPI Protocols

When operating in normal mode, the SPI bus internal address pointer is incremented depending upon which command has been transmitted. Multiple commands may be transmitted sequentually so long as the SPI_CS# pin is asserted low. Figure 3.1 shows an example of this operation.

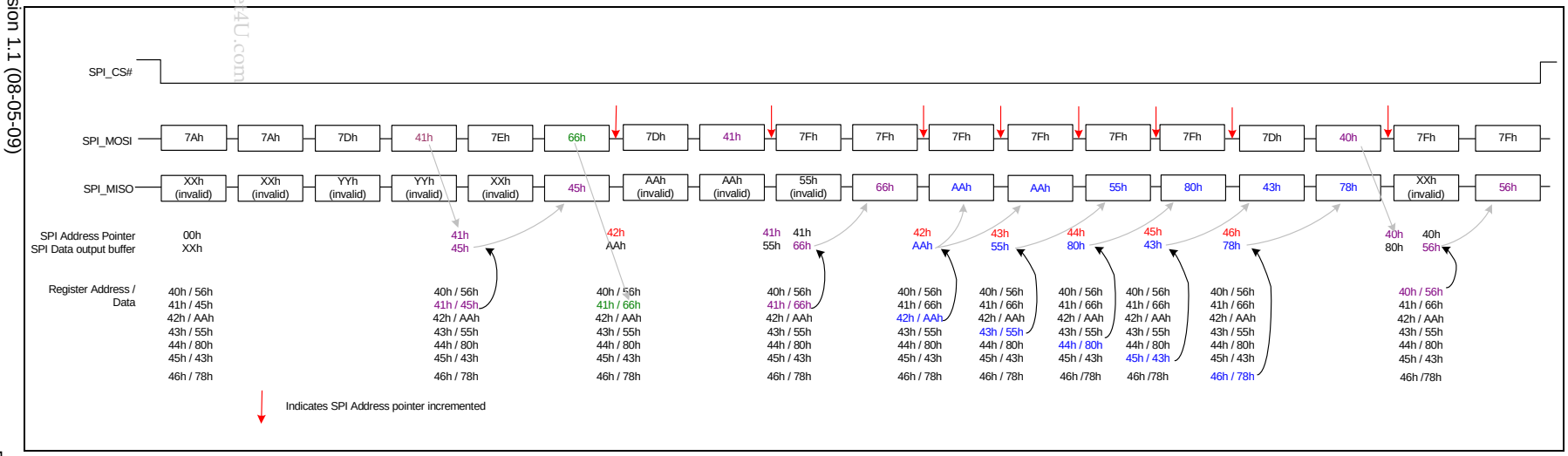


Figure 3.1 Example SPI Bus Communication - Normal Mode

3.5.1 Reset Interface

Resets the Serial interface whenever two successive 7Ah codes are received. Regardless of the current phase of the transaction - command or data, the receipt of the successive reset commands resets the Serial communication interface only. All other functions are not affected by the reset operation.

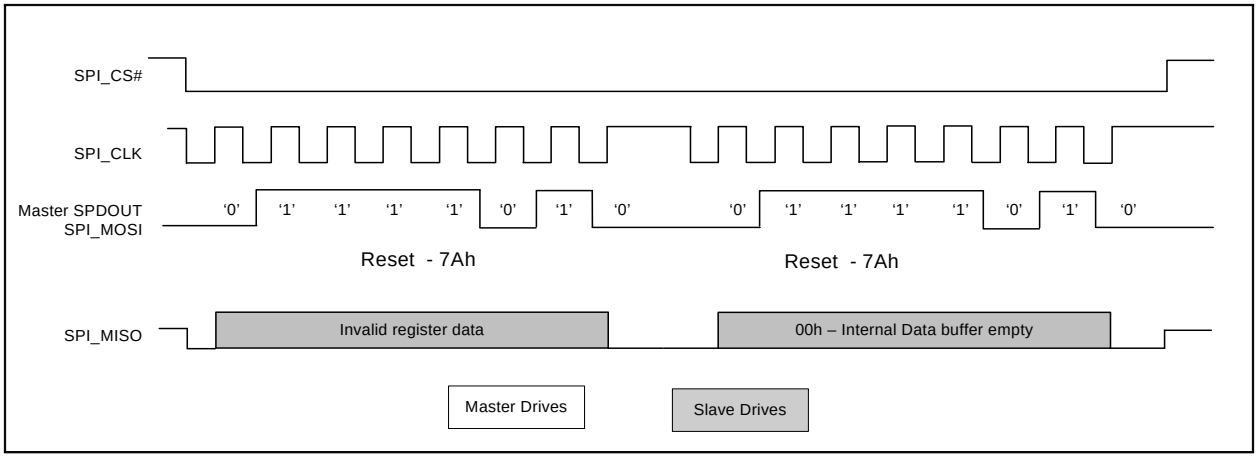


Figure 3.2 SPI Reset Interface Command - Normal Mode

3.5.2 Set Address Pointer

The Set Address Pointer command sets the Address pointer for subsequent reads and writes of data. The pointer is set on the rising edge of the final data bit. At the same time, the data that is to be read is fetched and loaded into the internal output buffer but is not transmitted.

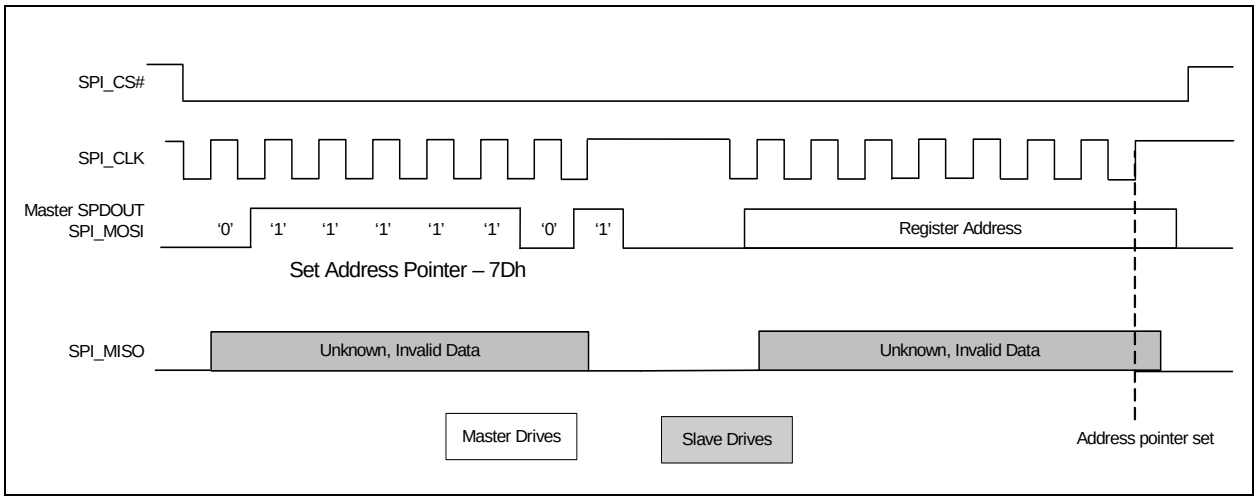


Figure 3.3 SPI Set Address Pointer Command - Normal Mode

3.5.3 Write Data

The Write Data protocol updates the contents of the register referenced by the address pointer. As the command is processed, the data to be read is fetched and loaded into the internal output buffer but not transmitted. Then, the register is updated with the data to be written. Finally, the address pointer is incremented.

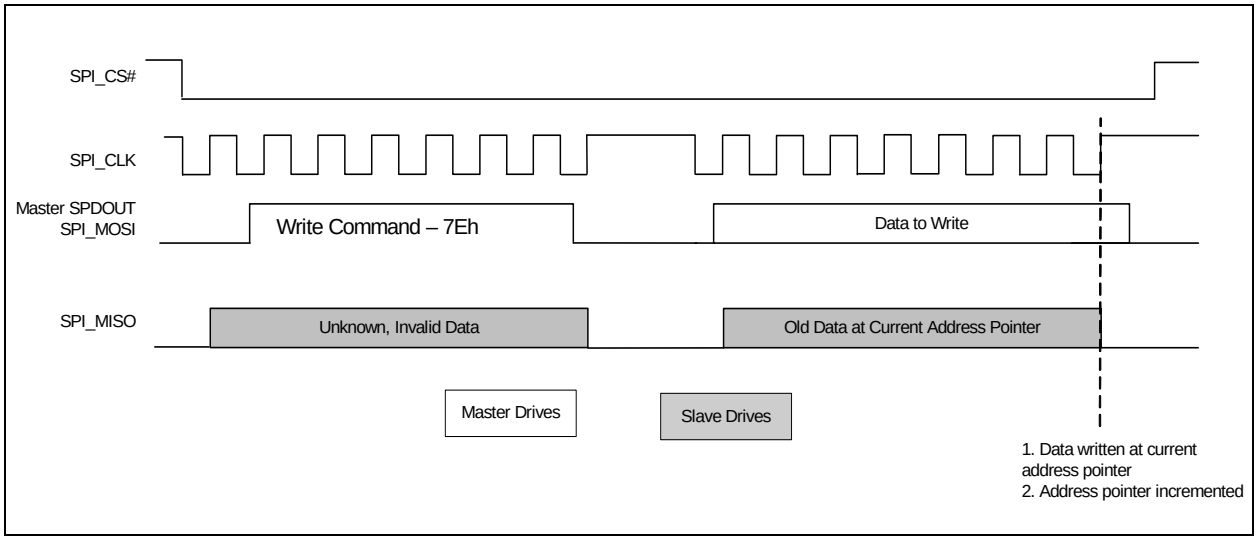


Figure 3.4 SPI Write Command - Normal Mode

3.5.4 Read Data

The Read Data protocol is used to read data from the device. During the normal mode of operation, while the device is receiving data, the CAP1005 is simultaneously transmitting data to the host. For the Set Address commands and the Write Data commands, this data may be invalid and it is recommended that the Read Data command is used.

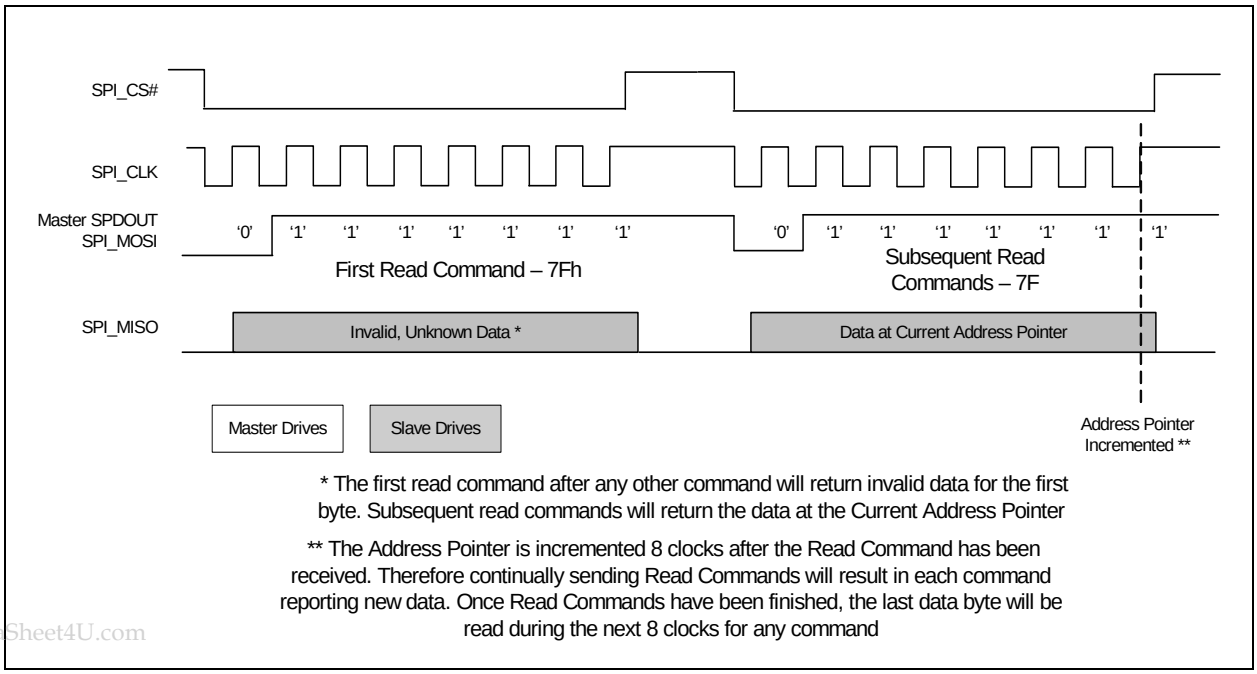


Figure 3.5 SPI Read Command - Normal Mode

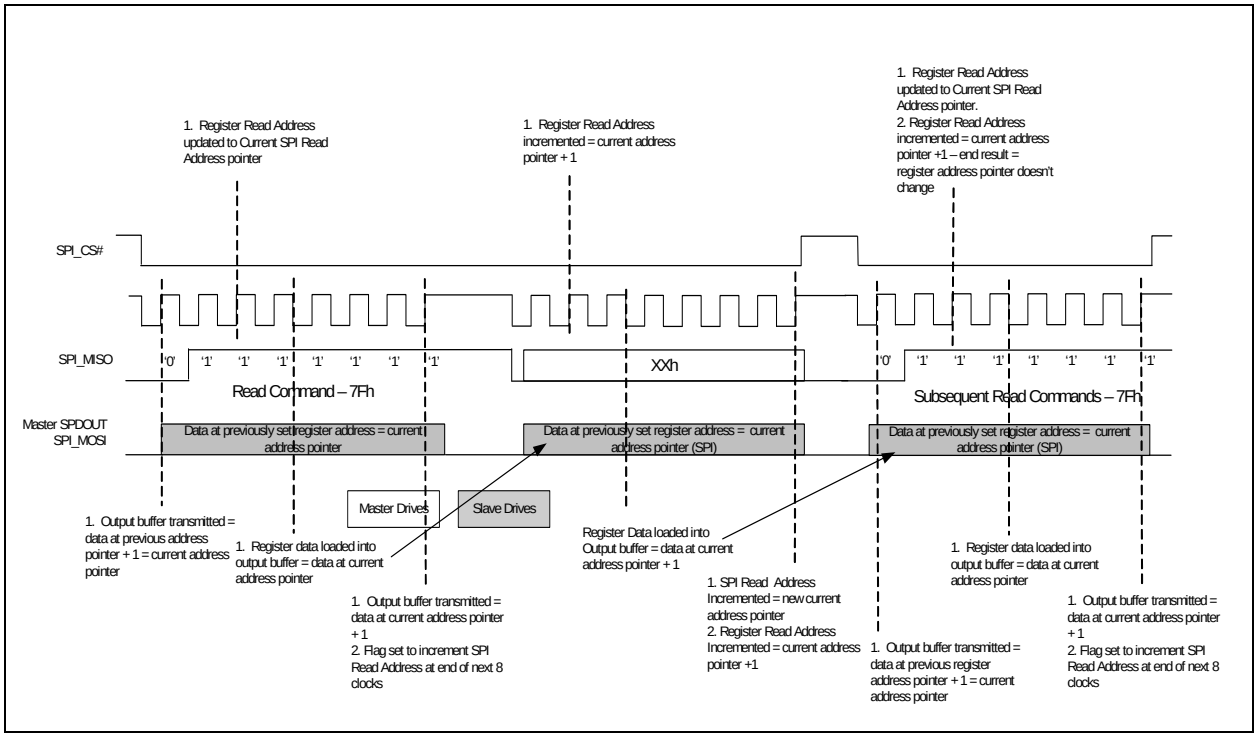


Figure 3.6 SPI Read Command - Normal Mode - Full

3.6 BC-Link Interface (CAP1006-2 only)

The BC-Link is a proprietary bus developed to allow communication between a host controller device to a companion device. This device uses this serial bus to read and write registers and for interrupt processing. The interface uses a data port concept, where the base interface has an address register, data register and a control register, defined in the SMSC's 8051's SFR space.

Refer to documentation for the BC-Link comptabile host controller for details on how to access the CAP1006 via the BC-Link Interface.

Chapter 4 General Description

The CAP1006 / 1005 are multiple channel Capacitive Touch sensors. The CAP1006 contains six (6) individual Capacitive Touch sensor inputs while the CAP1005 contains five (5) sensors. Both devices offer programmable sensitivity for use in touch sensor applications. Each sensor automatically recalibrates to compensate for gradual environmental changes.

The CAP1005 / CAP1006 offers multiple power states operating at low quiescent currents during its Deep Sleep state. It can monitor one or more channels while in a lower power state and respond to communications normally.

The device communicates with a host controller using the SPI bus (CAP1005 only), SMSC BC-Link bus (CAP1006-2 only), or via SMBus / I^2C (CAP1006-1 only). The host controller may poll the device for updated information at any time or it may configure the device to flag an interrupt whenever a touch is detected on any sensor.

A typical system diagram for the CAP1006 is shown in Figure 4.1 and a system diagram for the CAP1005 is shown in Figure 4.2.

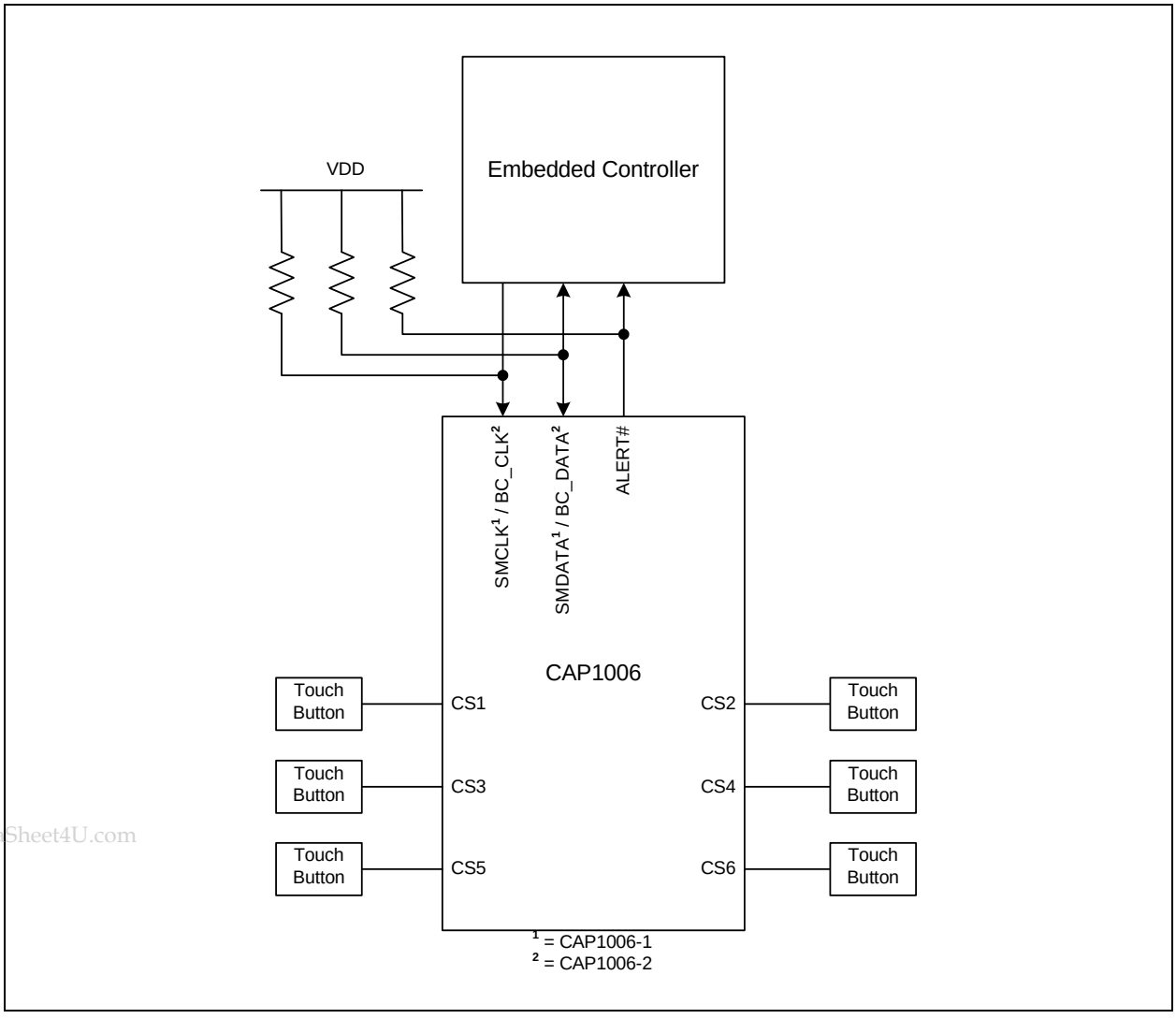


Figure 4.1 System Diagram for CAP1006

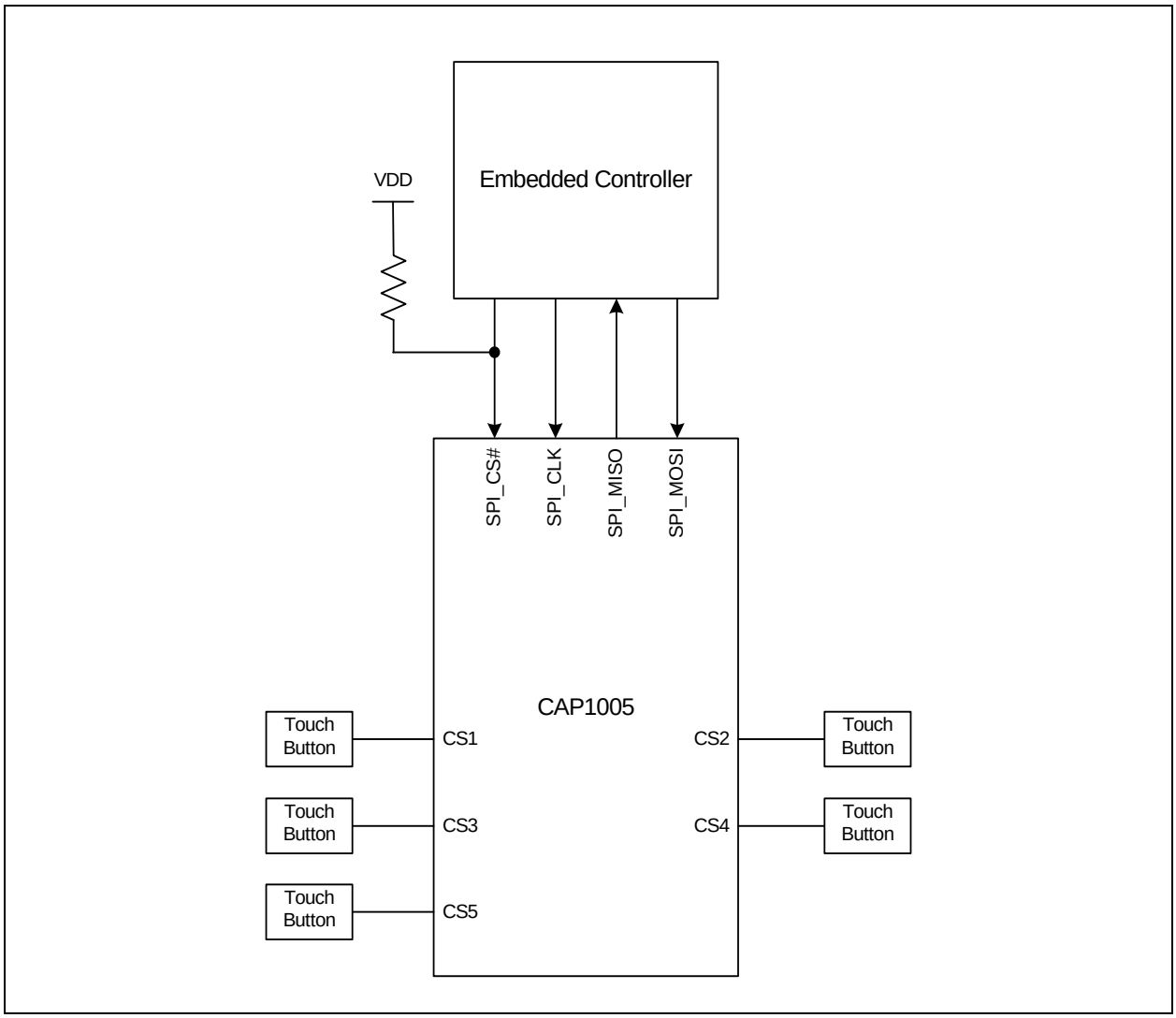


Figure 4.2 System Diagram for CAP1005

4.1 Power States

The CAP1005 / CAP1006 has three operating states depending on the status of the STBY and DSLEEP bits. When the device transitions between power states, previously detected touches (for inactive channels) are cleared and the status bits reset.

1. Fully Active - The device is fully active. It is monitoring all active Capacitive Sensor channels.
2. Standby - The device is in a lower power state. It will measure a programmable number of channels (as determined by the Standby Channel register - default none). Interrupts will still be generated based on the active channels. The device will still respond to communications normally and can be returned to the Fully Active state of operation by clearing the STBY bit.
3. Deep Sleep - The device is in its lowest power state. It is not monitoring any Capacitive Sensor channels. It can be awakened by SMBus or SPI communications targeting the device (which will cause the DSLEEP bit to be automatically cleared).

APPLICATION NOTE: The CAP1006-2, which communicates using the BC-Link protocol, does not support Deep Sleep.

4.2 Capacitive Touch Sensing

The CAP1005 / CAP1006 contains six (6) (CAP1006) or five (5) (CAP1005) independent Capacitive Touch Sensor inputs. Each sensor has dynamic range to detect a change of capacitance due to a touch. Additionally, each sensor can be configured to be automatically and routinely re-calibrated.

4.2.1 Sensing Cycle

Each Capacitive Touch Sensor has controls to be activated and included in the sensing cycle. When the device is active, it automatically initiates a sensing cycle and repeats the cycle every time it finishes. The cycle polls through each active Sensor starting with CS1 and extending through CS6. As each Capacitive Touch Sensor is polled, its measurement is compared against a baseline “not touched” measurement. If the delta measurement is large enough, then a touch is detected and an interrupt generated.

The sensing cycle time is programmable (see Section 5.10).

4.2.2 Recalibrating Sensors

Each sensor is regularly recalibrated at an adjustable rate. By default, the recalibration routine stores the average 256 previous measurements and periodically updates the base “Not Touched” setting for the Capacitive Touch Sensor input.

It is possible that the device loses sensitivity to a touch. This may happen as a result of a noisy environment, an accidental recalibration during a touch, or other environmental changes. When this occurs, then the base untouched sensor may generate negative delta count values. The device will detect this condition based on a programmable number of consecutive negative delta readings. When it detects the condition, the CAP1005 / CAP1006 will automatically re-calibrate the base-count settings. During this recalibration, the device will not respond to touches.

4.3 ALERT# Pin

The ALERT# pin is an active low output that is driven when an interrupt event is detected.

Whenever an interrupt is generated, the INT bit (see Section 5.1) is set. The ALERT# pin is cleared when INT bit is cleared by the user. Additionally, when the INT bit is cleared by the user, status bits are only cleared if no touch is detected.

4.3.1 Sensor Interrupt Behavior

The sensor interrupts are generated in one of two ways:

1. An interrupt is generated when a touch is detected and when a release is detected (see Figure 4.4).
2. If the repeat rate is enabled (see Section 5.6), then, so long as the touch is held, another interrupt will be generated based on the programmed repeat rate (see Figure 4.3).

When the repeat rate is enabled, the device uses an additional control called MPRESS that determines whether a touch is flagged as a simple “touch” or a “press and hold”. The MPRESS[3:0] bits set a minimum press timer. When the button is touched the timer begins. If the sensor is released before the minimum press timer expires, then it is flagged as a touch and an interrupt is generated upon the release. If the sensor detects a touch for longer than this timer value, then it is flagged as a “press and hold” event. So long as the touch is held, interrupts will be generated at the programmed repeat rate and upon a release.

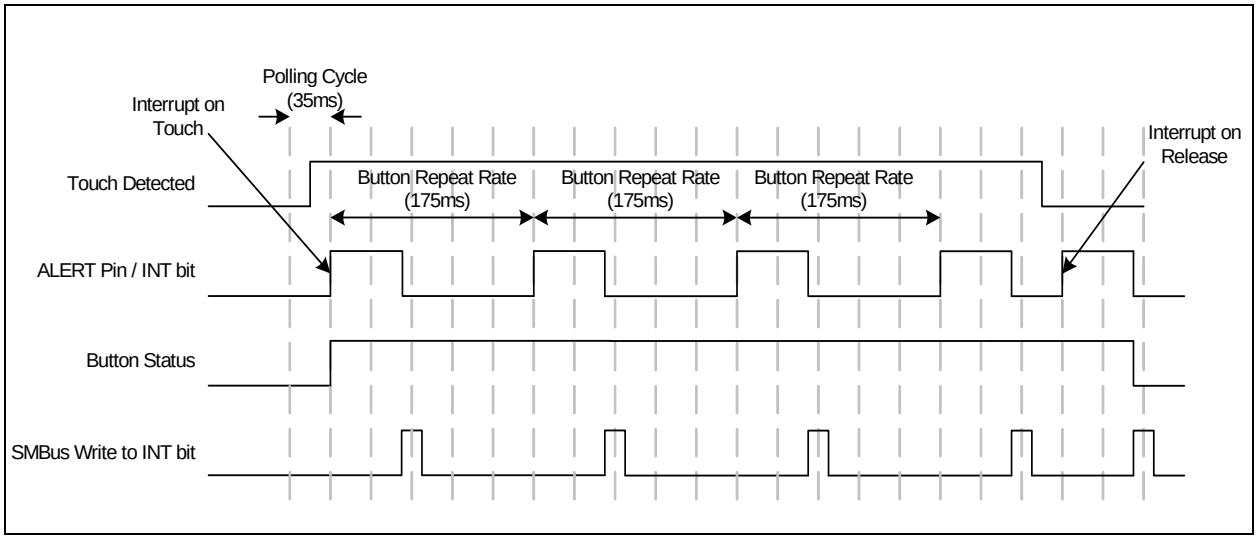


Figure 4.3 Sensor Interrupt Behavior - Repeat Rate Enabled

APPLICATION NOTE: The host may need to poll the device twice to determine that a release has been detected.

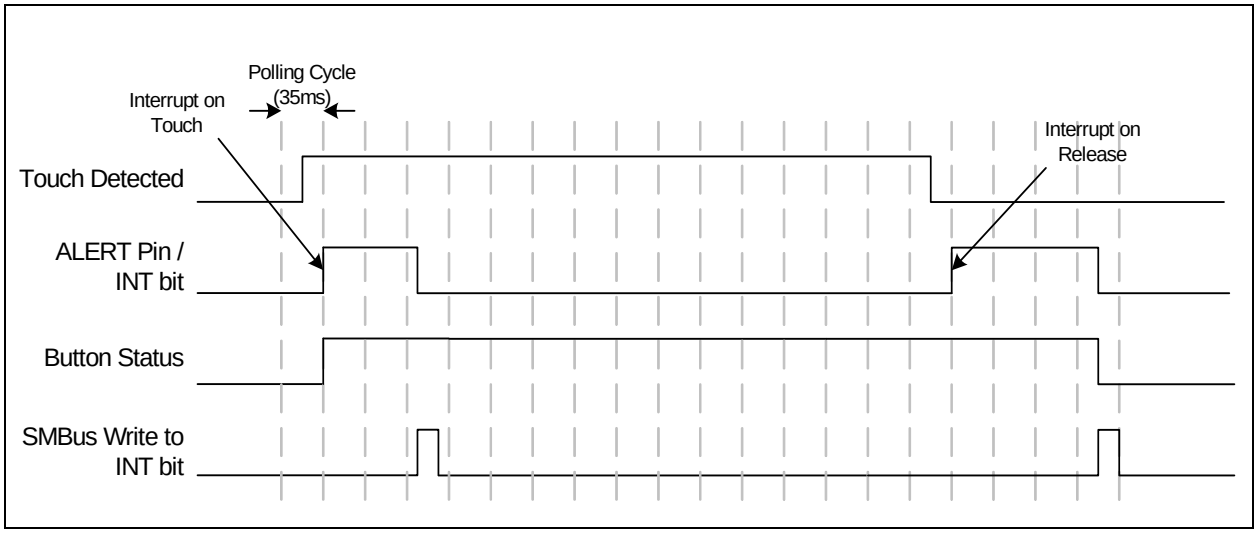


Figure 4.4 Sensor Interrupt Behavior - No Repeat Rate Enabled

Chapter 5 Register Description

The registers shown in Table 5.1 are accessible through the communications protocol. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R/W	Main Status Control	Controls general power states and power dissipation	00h	Page 29
03h	R	Sensor Status	Returns the state of the sampeld Capacative Touch Sensor	00h	Page 30
0Ah	R	Noise Flag Status	Stores the noise flags for sensors	00h	Page 30
10h	R	Sensor 1 Delta Count	Stores the delta count for CS1	00h	Page 31
11h	R	Sensor 2 Delta Count	Stores the delta count for CS2	00h	Page 31
12h	R	Sensor 3 Delta Count	Stores the delta count for CS3	00h	Page 31
13h	R	Sensor 4 Delta Count	Stores the delta count for CS4	00h	Page 31
14h	R	Sensor 5 Delta Count	Stores the delta count for CS5	00h	Page 31
15h	R	Sensor 6 Delta Count	Stores the delta count for CS6	00h	Page 31
1Fh	R/W	Sensitivity Control	Controls the sensitivity of the threshold and delta counts and data scaling of the base counts	2Fh	Page 31
20h	R/W	Configuration	Controls general functionality	20h	Page 33
21h	R/W	Sensor Enable	Controls whether the Capacitive Touch Sensor inputs are sampled	3Fh	Page 33
22h	R/W	Sensor Configuration	Controls reset delay and auto-repeat delay for sensors operating in the full power state	A4h	Page 34
23h	R/W	Sensor Configuration 2	Controls the MPRESS controls for all sensors	07h	Page 36
24h	R/W	Averaging and Sampling Config	Controls averaging and sampling window	1Dh	Page 36
26h	R/W	Calibration Activate	Activates manual re-calibration for Capacative Touch Sensors	FFh	Page 38
27h	R/W	Interrupt Enable	Enables Interrupts associated with Capacative Touch Sensors	3Fh	Page 38
28h	R/W	Repeat Rate Enable	Enables repeat rate for Capacative Touch Sensors	3Fh	Page 39
2Ah	R/W	Multiple Press Configuration	Determines the number of simultaneous touches to flag a multiple touch condition	80h	Page 39
2Fh	R/W	Recalibration Configuration	Determines re-calibration timing and sampling window	8Bh	Page 40

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
30h	R/W	Sensor 1 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 1	40h	Page 41
31h	R/W	Sensor 2 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 2	40h	Page 41
32h	R/W	Sensor 3 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 3	40h	Page 41
33h	R/W	Sensor 4 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 4	40h	Page 41
34h	R/W	Sensor 5 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 5	40h	Page 41
35h	R/W	Sensor 6 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 6	40h	Page 41
38h	R/W	Sensor Noise Threshold 1	Stores controls for selecting the noise threshold for sensors 1 - 4	55h	Page 42
39h	R/W	Sensor Noise Threshold 2	Stores controls for selecting the noise threshold for sensors 5 - 6	55h	Page 42
Standby Configuration Registers					
40h	R/W	Standby Channel	Controls which sensors are enabled while in standby	00h	Page 43
41h	R/W	Standby Configuration	Controls averaging and cycle time while in standby	1Dh	Page 43
42h	R/W	Standby Sensitivity	Controls sensitivity settings used while in standby	02h	Page 45
43h	R/W	Standby Threshold	Stores the touch detection threshold for active sensors in standby	40h	Page 45
50h	R	Sensor 1 Base Count	Stores the reference count value for sensor 1	C8h	Page 46
51h	R	Sensor 2 Base Count	Stores the reference count value for sensor 2	C8h	Page 46
52h	R	Sensor 3 Base Count	Stores the reference count value for sensor 3	C8h	Page 46
53h	R	Sensor 4 Base Count	Stores the reference count value for sensor 4	C8h	Page 46
54h	R	Sensor 5 Base Count	Stores the reference count value for sensor 5	C8h	Page 46
55h	R	Sensor 6 Base Count	Stores the reference count value for sensor 6	C8h	Page 46

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
FDh	R	Product ID CAP1006	Stores a fixed value that identifies each product	44h	Page 46
		Product ID CAP1005	Stores a fixed value that identifies each product	45h	
FEh	R	Manufacturer ID	Stores a fixed value that identifies SMSC	5Dh	Page 47
FFh	R	Revision	Stores a fixed value that represents the revision number	81h	Page 47

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

5.1 Main Status Control Register

Table 5.2 Main Status Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R/W	Main Status Control	-	-	STBY	DSLEEP	-	-	-	INT	00h

The Main Status and Control register controls the primary power state of the device.

Bit 5 - STBY - Enables Standby.

- ‘0’ (default) - Sensor scanning is active.
- ‘1’ - Capacitive Touch Sensor scanning is limited to the sensors set in the Standby Channel register (see Section 5.18). The status registers will not be cleared until read. Sensors that are no longer sampled will flag a release and then remain in a non-touched state.

Bit 4 - DSLEEP - Enables Deep Sleep by deactivating all functions. This bit will be cleared when SPI or SMBus are received targeting the CAP1005 / CAP1006. If the CAP1005 / CAP1006 is configured to communicate using the BC-Link protocol, then this bit is ignored.

- ‘0’ (default) - Sensor scanning is active.
- ‘1’ - All sensor scanning is disabled. The status registers are automatically cleared and the INT bit is cleared.

Bit 0 - INT - Indicates that there is an interrupt. This bit is only set if the ALERT# pin has been asserted. If a channel detects a touch and its associated interrupt enable bit is not set to a logic ‘1’ then no action is taken.

This bit is cleared by writing a logic ‘0’ to it. When this bit is cleared, the ALERT# pin will be deasserted and all status registers will be cleared if the condition has been removed. If the WAKE/SPI_MOSI pin is asserted as a result of a touch detected while in Standby, it will likewise be deasserted when this bit is cleared.

Note that this pin is not driven when communicating via the 4-wire SPI protocol

- ‘0’ - No interrupt pending.

- '1' - A touch has been detected on one or more channels and the interrupt has been asserted.

5.2 Status Registers

Table 5.3 Status Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R	Sensor Status	-	-	CS6	CS5	CS4	CS3	CS2	CS1	00h

The Sensor Status Registers store status bits that indicate a touch has been detected. A value of '0' in any bit indicates that no touch has been detected. A value of '1' in any bit indicates that a touch has been detected.

All status bits are cleared when the device enters the Deep Sleep (DSLEEP = '1' - see Section 5.1). All status bits are cleared when the INT bit is cleared and if a touch on the respective Capacitive Touch Sensor is no longer present. If a touch is still detected, then the bits will not be cleared (but this will not cause the interrupt to be asserted - see Section 5.6).

Bit 5 - CS6 - Indicates that a touch was detected on Sensor 6.

Bit 4 - CS5 - Indicates that a touch was detected on Sensor 5.

Bit 3 - CS4 - Indicates that a touch was detected on Sensor 4.

Bit 2 - CS3 - Indicates that a touch was detected on Sensor 3.

Bit 1 - CS2 - Indicates that a touch was detected on Sensor 2.

Bit 0 - CS1 - Indicates that a touch was detected on Sensor 1.

5.3 Noise Flag Status Registers

Table 5.4 Noise Flag Status Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ah	R	Noise Flag Status	-	-	CS6_ NOISE	CS5_ NOISE	CS4_ NOISE	CS3_ NOISE	CS2_ NOISE	CS1_ NOISE	00h

The Noise Flag Status registers store status bits that are generated from the analog block if the detected noise is above the operating region of the analog detector. These bits indicate that the most recently received data from the sensor is invalid and should not be used for touch detection. Furthermore, so long as the bit is set for a particular channel, no decisions are made with the data. A touch is not detected, and a release is not detected.

These bits are not sticky and will be cleared automatically if the analog block does not report a noise error.

5.4 Sensor Delta Count Registers

Table 5.5 Sensor Delta Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
10h	R	Sensor 1 Delta Count	Sign	64	32	16	8	4	2	1	00h
11h	R	Sensor 2 Delta Count	Sign	64	32	16	8	4	2	1	00h
12h	R	Sensor 3 Delta Count	Sign	64	32	16	8	4	2	1	00h
13h	R	Sensor 4 Delta Count	Sign	64	32	16	8	4	2	1	00h
14h	R	Sensor 5 Delta Count	Sign	64	32	16	8	4	2	1	00h
15h	R	Sensor 6 Delta Count	Sign	64	32	16	8	4	2	1	00h

The Sensor Delta Count registers store the delta count that is compared against the threshold used to determine if a touch has been detected. The count value represents a change in input due to the capacitor associated with a touch on one of the sensors and is referenced to a calibrated base “Not touched” count value. The delta is an instantaneous change and is updated once per sensor per sensing cycle (see Section 4.2.1 - sensor cycle).

The value presented is a standard 2’s complement number. In addition, the value is capped at a value of 7Fh. A reading of 7Fh indicates that the sensitivity settings are too high and should be adjusted accordingly (see Section 5.5).

The value is also capped at a negative value of FFh for negative delta counts which may result upon a release.

5.5 Sensitivity Control Register

Table 5.6 Sensitivity Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Sensitivity Control	-	DELTA_SENSE[2:0]			BASE_SHIFT[3:0]				2Fh

The Sensitivity Control register controls the sensitivity of a touch detection.

Bits 6- 4 DELTA_SENSE[2:0] - Controls the sensitivity of a touch detection. The sensitivity settings act to scale the relative delta count value higher or lower based on the system parameters. A setting of 000b is the most sensitive while a setting of 111b is the least sensitive. At the more sensitive settings, touches are detected for a smaller delta C corresponding to a “lighter” touch. These settings are more sensitive to noise however and a noisy environment may flag more false touches than higher sensitivity levels.

APPLICATION NOTE: A value of 128x is the most sensitive setting available. At the most sensitivity settings, the MSB of the Delta Count register represents 64 out of ~25,000 which corresponds to a touch of approximately 0.25% of the base capacitance (or a ΔC of 25fF from a 10pF base capacitance). Conversely a value of 1x is the least sensitive setting available. At these

settings, the MSB of the Delta Count register corresponds to a delta count of 8192 counts out of ~25,000 which corresponds to a touch of approximately 33% of the base capacitance (or a ΔC of 3.33pF from a 10pF base capacitance).

Table 5.7 DELTA_SENSE Bit Decode

DELTA_SENSE[2:0]			SENSITIVITY MULTIPLIER
2	**1**	**0**	
0	0	0	128x (most sensitive)
0	0	1	64x
0	1	0	32x (default)
0	1	1	16x
1	0	0	8x
1	0	1	4x
1	1	0	2x
1	1	1	1x - (least sensitive)

Bits 3 - 0 - BASE_SHIFT[3:0] - Controls the scaling and data presentation of the Base Count registers. The higher the value of these bits, the larger the range and the lower the resolution of the data presented. The scale factor represents the multiplier to the bit-weighting presented in these register descriptions.

APPLICATION NOTE: The BASE_SHIFT[3:0] bits normally do not need to be updated. These settings will not affect touch detection or sensitivity. These bits are sometimes helpful in analyzing the Cap Sensing board performance and stability.

Table 5.8 BASE_SHIFT Bit Decode

BASE_SHIFT[3:0]				DATA SCALING FACTOR
3	**2**	**1**	**0**	
0	0	0	0	1x
0	0	0	1	2x
0	0	1	0	4x
0	0	1	1	8x
0	1	0	0	16x
0	1	0	1	32x
0	1	1	0	64x
0	1	1	1	128x
1	0	0	0	256x
All others				256x (default = 1111b)

5.6 Configuration Register

Table 5.9 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	R/W	Configuration	TIMEOUT	-	BLK_ DIG_ NOISE	BLK_ ANA_ NOISE	MAX_DUR_ EN	-	-	-	20h

The Configuration register controls general global functionality that affects the entire device.

Bit 7 - TIMEOUT - Enables the timeout and idle functionality of the SMBus protocol.

- '0' (default) - The SMBus timeout and idle functionality are disabled. The SMBus interface will not time out if the clock line is held low. Likewise, it will not reset if both the data and clock lines are held high for longer than 150us. This is used for I^2C compliance.
- '1' - The SMBus timeout and idle functionality are enabled. The SMBus interface will time out if the clock line is held low for longer than 30ms. Likewise, it will reset if both the data and clock lines are held high for longer than 150us.

Bit 5 - BLK_DIG_NOISE - Determines whether the digital noise threshold is used by the device.

- '0' - The digital noise threshold is used. If a delta count value exceeds the noise threshold but does not exceed the touch threshold, then the sample is discarded and not used for the automatic re-calibration routine.
- '1' (default) - The noise threshold is not used. Any delta count that is less than the touch threshold is used for the automatic re-calibration routine.

Bit 4 - BLK_ANA_NOISE - Determines whether the analog noise flag setting will block a touch detection as well as the analog calibration routine.

- '0' (default) - If the analog noise bit is set, then a touch is blocked on the corresponding channel and will force the analog calibration routine to retry.
- '1' - A touch is not blocked even if the analog noise bit is set. Likewise, the analog calibration routine will not retry if the analog noise bit is set.

Bit 3 - MAX_DUR_EN - Determines whether the maximum duration recalibration is enabled for non-grouped sensors.

- '0' (default) - The maximum duration recalibration functionality is disabled. A touch may be held indefinitely and no re-calibration will be performed on any sensor.
- '1' - The maximum duration recalibration functionality is enabled. If a touch is held for longer than the MAX_DUR bit settings, then the re-calibration routine will be restarted (see Section 5.8).

5.7 Sensor Enable Registers

Table 5.10 Sensor Enable Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	Sensor Enable	-	-	CS6_EN	CS5_EN	CS4_EN	CS3_EN	CS2_EN	CS1_EN	3Fh

The Sensor Enable registers determine whether a Capacitive Touch Sensor input is included in the sampling cycle. The length of the sampling cycle is not affected by the number of sensors measured.

Bit 5 - CS6_EN - Enables the CS6 input to be included during the sampling cycle.

- '0' - The CS6 input is not included in the sampling cycle.

- ‘1’ (default) - The CS6 input is included in the sampling cycle.

Bit 4 - CS5_EN - Enables the CS5 input to be included during the sampling cycle.

Bit 3 - CS4_EN - Enables the CS4 input to be included during the sampling cycle.

Bit 2 - CS3_EN - Enables the CS3 input to be included during the sampling cycle.

Bit 1 - CS2_EN - Enables the CS2 input to be included during the sampling cycle.

Bit 0 - CS1_EN - Enables the CS1 input to be included during the sampling cycle.

5.8 Sensor Configuration Register

Table 5.11 Sensor Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Sensor Configuration	MAX_DUR[3:0]				RPT_RATE[3:0]				A4h

The Sensor Configuration Register controls timings associated with the Capacitive Sensor channels 1 - 6.

Bits 7 - 4 - MAX_DUR[3:0] - (default 1010b) - Determines the maximum time that a sensor is allowed to be touched until the Capacitive Touch sensor is recalibrated as shown in Table 5.12.

Table 5.12 MAX_DUR Bit Decode

MAX_DUR[3:0]				TIME BEFORE RECALIBRATION
3	**2**	**1**	**0**	
0	0	0	0	560ms
0	0	0	1	840ms
0	0	1	0	1120ms
0	0	1	1	1400ms
0	1	0	0	1680ms
0	1	0	1	2240ms
0	1	1	0	2800ms
0	1	1	1	3360ms
1	0	0	0	3920ms
1	0	0	1	4480ms
1	0	1	0	5600ms
1	0	1	1	6720ms
1	1	0	0	7840ms
1	1	0	1	8906ms
1	1	1	0	10080ms
1	1	1	1	11200ms

Bits 3 - 0 - RPT_RATE[3:0] - (default 0100b) Determines the time duration between interrupt assertions when auto repeat is enabled. The resolution is 35ms the range is from 35ms to 560ms as shown in Table 5.13.

Table 5.13 RPT_RATE Bit Decode

RPT_RATE[3:0] OR M_PRESS[3:0]				INTERRUPT REPEAT RATE OR M_PRESS TIME
3	**2**	**1**	**0**	
0	0	0	0	35ms
0	0	0	1	70ms
0	0	1	0	105ms
0	0	1	1	140ms
0	1	0	0	175ms
0	1	0	1	210ms
0	1	1	0	245ms

Table 5.13 RPT_RATE Bit Decode (continued)

RPT_RATE[3:0] OR M_PRESS[3:0]				INTERRUPT REPEAT RATE OR M_PRESS TIME
3	2	1	0	
0	1	1	1	280ms
1	0	0	0	315ms
1	0	0	1	350ms
1	0	1	0	385ms
1	0	1	1	420ms
1	1	0	0	455ms
1	1	0	1	490ms
1	1	1	0	525ms
1	1	1	1	560ms

5.9 Sensor Configuration 2 Register

Table 5.14 Sensor Configuration 2 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
23h	R/W	Sensor Configuration 2	-	-	-	-	M_PRESS[3:0]				07h

Bits 3- 0 - M_PRESS[3:0] - (default 0111b) - Determines the minimum amount of time that sensors configured to use auto repeat must detect a sensor touch to detect a “press and hold” event. If the sensor detects a touch for longer than the M_PRESS[3:0] settings, then a “press and hold” event is detected.

This is the maximum amount of time that sensors can detect a sensor touch to differentiate between a “touch” and a “press and hold”. If a sensor detects a touch for less than or equal to the M_PRESS[3:0] settings, then a touch event is detected.

The resolution is 35ms the range is from 35ms to 560ms as shown in Table 5.13.

5.10 Averaging and Sampling Configuration Register

Table 5.15 Averaging and Sampling Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
24h	R/W	Averaging and Sampling Config			AVG[2:0]			SAMP_ TIME	CYCLE_TIME [1:0]		1Dh

The Averaging and Sampling Configuration register controls the number of samples taken and the total sensor cycle time for all active sensors while the device is functioning normally.

Bits 5 - 3 - AVG[2:0] - Determines the number of samples that are taken for all active channels during the sensor cycle as shown in Table 5.16. All samples are taken consecutively on the same channel

before the next channel is sampled and the result is averaged over the number of samples measured before updating the measured results.

For example, if CS1, CS2, and CS3 are sampled during the sensor cycle, and the AVG[2:0] bits are set to take 4 samples per channel, then the full sensor cycle will be: CS1, CS1, CS1, CS1, CS2, CS2, CS2, CS2, CS3, CS3, CS3, CS3.

Table 5.16 AVG Bit Decode

AVG[2:0]			NUMBER OF SAMPLES TAKEN PER MEASUREMENT
2	**1**	**0**	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8 (default)
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Bit 2 - SAMP_TIME - Determines the time to take a single sample.

- '0' - The sampling time is ~2.56ms.
- '1' (default) - The sampling time is ~1.28ms.

Bits 1 - 0 - CYCLE_TIME[1:0] - Determines the overall cycle time for all measured channels during normal operation as shown in Table 5.17. All measured channels are sampled at the beginning of the cycle time. If additional time is remaining, then the device is placed into a lower power state for the remaining duration of the cycle.

Table 5.17 CYCLE_TIME Bit Decode

CYCLE_TIME[1:0]		OVERALL CYCLE TIME
1	**0**	
0	0	35ms
0	1	70ms (default)
1	0	105ms
1	1	140ms

APPLICATION NOTE: The programmed cycle time is only maintained if the total averaging time for all samples is less than the programmed cycle. The AVG[2:0] bits will take priority so that if more samples are required than would normally be allowed during the cycle time, the cycle time will be extended as necessary to accommodate the number of samples to be measured.

5.11 Calibration Activate Registers

Table 5.18 Calibration Activate Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
26h	R/W	Calibration Activate	-	-	CS6_CAL	CS5_CAL	CS4_CAL	CS3_CAL	CS2_CAL	CS1_CAL	FFh

The Calibration Activate register force the respective sensors to be re-calibrated. When a bit is set, the corresponding Capacitive Touch Sensor will be re-calibrated and the bit will be automatically cleared once the re-calibration routine has finished. During the re-calibration routine, the sensors will not detect a press for up to 600ms and the Sensor Base Count register values will be invalid. During this time, any press on the corresponding sensors will invalidate the re-calibration.

Bit 5 - CS6_CAL - When set, the CS6 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 4 - CS5_CAL - When set, the CS5 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 3 - CS4_CAL - When set, the CS4 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 2 - CS3_CAL - When set, the CS3 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 1 - CS2_CAL - When set, the CS2 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 0 - CS1_CAL - When set, the CS1 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

5.12 Interrupt Enable Register

Table 5.19 Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R/W	Interrupt Enable	-	-	CS6_ INT_EN	CS5_ INT_EN	CS4_ INT_EN	CS3_ INT_EN	CS2_ INT_EN	CS1_ INT_EN	3Fh

The Interrupt Enable registers determine whether a sensor touch or release causes the interrupt pin to be asserted.

Bit 5 - CS6_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS6 (associated with the CS6 status bit).

- ‘0’ - The interrupt pin will not be asserted if a touch is detected on CS6 (associated with the CS6 status bit).
- ‘1’ (default) - The interrupt pin will be asserted a touch is detected on CS6 (associated with the CS6 status bit).

Bit 4 - CS5_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS5 (associated with the CS5 status bit).

Bit 3 - CS4_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS4 (associated with the CS4 status bit).

Bit 2 - CS3_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS3 (associated with the CS3 status bit).

Bit 1 - CS2_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS2 (associated with the CS2 status bit).

Bit 0 - CS1_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS1 (associated with the CS1 status bit).

5.13 Repeat Rate Enable Register

Table 5.20 Repeat Rate Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
28h	R/W	Repeat Rate Enable	-	-	CS6_RPT_EN	CS5_RPT_EN	CS4_RPT_EN	CS3_RPT_EN	CS2_RPT_EN	CS1_RPT_EN	3Fh

The Repeat Rate Enable register determines the interrupt behavior of the buttons as described in Section 4.3.1.

Bit 5 - CS6_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 6.

- '0' - The repeat rate for CS6 is disabled. It will only generate an interrupt when a touch is detected and when a release is detected no matter how long the touch is held for.
- '1' (default) - The repeat rate for CS6 is enabled. In the case of a "touch" event, it will generate an interrupt when a touch is detected and a release is detected. In the case of a "press and hold" event, it will generate an interrupt when a touch is detected and at the repeat rate so long as the touch is held. It will not generate an interrupt when a release is detected.

Bit 4 - CS5_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 5.

Bit 3 - CS4_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 4.

Bit 2 - CS3_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 3.

Bit 1 - CS2_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 2.

Bit 0 - CS1_RPT_EN - Enables the repeat rate for Capacitive Touch Sensor 1.

5.14 Multiple Touch Configuration Register

Table 5.21 Multiple Touch Configuration

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ah	R/W	Multiple Touch Config	MULT_BLK_EN	-	-	-	B_MULT_T[1:0]		-	-	80h

The Multiple Touch Configuration register controls the settings for the multiple touch detection circuitry. These settings determine the number of simultaneous buttons that may be pressed before action is taken.

Bit 7 - MULT_BLK_EN - Enables the multiple button blocking circuitry.

- '0' - The multiple touch circuitry is disabled. The device will not block multiple touches.
- '1' (default)- The multiple touch circuitry is enabled. The device will accept the number of touches equal to programmed multiple touch threshold and block all others. It will remember which sensor is valid and block all others until that sensor has been released.

Bits 3 - 2 - B_MULT_T[1:0] - Determines the number of simultaneous touches on all sensors before a Multiple Touch Event is detected and sensors are blocked. The bit decode is given by Table 5.22.

Table 5.22 B_MULT_T Bit Decode

B_MULT_T[1:0]		NUMBER OF SIMULTANEOUS TOUCHES
1	**0**	
0	0	1 (default)
0	1	2
1	0	3
1	1	4

5.15 Recalibration Configuration Register

Table 5.23 Recalibration Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Fh	R/W	Recalibration Configuration	BUT_ LD_TH	-	-	NEG_DELTA_ CNT[1:0]		CAL_CFG[2:0]			8Bh

The Recalibration Configuration register controls the automatic re-calibration routine settings as well as advanced controls to program the Sensor Threshold register settings.

Bit 7 - BUT_LD_TH - Enables setting all Sensor Threshold registers by writing to the Sensor 1 Threshold register.

- '0' - Each Sensor X Threshold register is updated individually.
- '1' (default) - Writing the Sensor 1 Threshold register will automatically overwrite the Sensor Threshold registers for all sensors (Sensor Threshold 1 through Sensor Threshold 6). The individual Sensor X Threshold registers (Sensor 2 Threshold through Sensor 6 Threshold) can be individually updated at any time.

Bits 4 - 3 - NEG_DELTA_CNT[1:0] - Determines the number of negative delta counts necessary to trigger a digital re-calibration as shown in Table 5.24.

Table 5.24 NEG_DELTA_CNT Bit Decode

NEG_DELTA_CNT[1:0]		NUMBER OF CONSECUTIVE NEGATIVE DELTA COUNT VALUES
1	**0**	
0	0	8
0	1	16 (default)
1	0	32
1	1	None (disabled)

Bits 2 - 0 - CAL_CFG[2:0] - Determines the update time and number of samples of the automatic re-calibration routine. The settings applies to all sensors universally (though individual sensors can be configured to support re-calibration - see Section 5.11).

Table 5.25 CAL_CFG Bit Decode

CAL_CFG[2:0]			RECALIBRATION SAMPLES (SEE Note 5.1)	UPDATE TIME (SEE Note 5.2)
2	**1**	**0**		
0	0	0	16	16
0	0	1	32	32
0	1	0	64	64
0	1	1	256	256 (default)
1	0	0	256	1024
1	0	1	256	2048
1	1	0	256	4096
1	1	1	256	7936

Note 5.1 Recalibration Samples refers to the number of samples that are measured and averaged before the Base Count is updated however does not control the base count update period. Once this target number of update cycles is reached, the device may wait additional time as determined by the Update Time before the base count is updated as determiend by the settings.

Note 5.2 Update Time refers to the amount of time (in polling cycle periods) that elapses before the Base Count is updated. For those settings that have the Update Time greater than the Recalibration Samples value, the device will wait (and continue to average the updated base count) until the Update Time has elapsed before the base count is updated.

5.16 Sensor Threshold Registers

Table 5.26 Sensor Threshold Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	Sensor 1 Threshold	-	64	32	16	8	4	2	1	40h
31h	R/W	Sensor 2 Threshold	-	64	32	16	8	4	2	1	40h
32h	R/W	Sensor 3 Threshold	-	64	32	16	8	4	2	1	40h
33h	R/W	Sensor 4 Threshold	-	64	32	16	8	4	2	1	40h
34h	R/W	Sensor 5 Threshold	-	64	32	16	8	4	2	1	40h
35h	R/W	Sensor 6 Threshold	-	64	32	16	8	4	2	1	40h

The Sensor Threshold registers store the delta threshold that is used to determine if a touch has been detected. When a touch occurs, the input signal of the corresponding sensor changes due to the capacitance associated with a touch. If the sensor input change exceeds the threshold settings, then a touch is detected.

When the BUT_LD_TH bit is set (see Section 5.15 - bit 7), writing data to the Sensor 1 Threshold register will update all of the sensor threshold registers (31h - 37h inclusive).

5.17 Sensor Noise Threshold Registers

Table 5.27 Sensor Noise Threshold Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
38h	R/W	Sensor Noise Threshold 1	CS4_BN_TH [1:0]		CS3_BN_TH [1:0]		CS2_BN_TH [1:0]		CS1_BN_TH [1:0]		55h
39h	R/W	Sensor Noise Threshold 2	0	1	0	1	CS6_BN_TH [1:0]		CS5_BN_TH [1:0]		55h

The Sensor Noise Threshold registers control the value of a secondary internal threshold to detect noise and improve the automatic recalibration routine. If a Capacitive Touch Sensor output exceeds the Sensor Noise Threshold but does not exceed the sensor threshold, then it is determined to be caused by a noise spike. That sample is not used by the automatic re-calibration routine.

The Sensor Noise Threshold is proportional to the programmed threshold as shown in Table 5.28.

Table 5.28 CSx_BN_TH Bit Decode

CSX_BN_TH[1:0]		THRESHOLD DIVIDE SETTING
1	**0**	
0	0	25%
0	1	37.5% (default)
1	0	50%
1	1	62.5%

5.17.1 Sensor Noise Threshold 1 Register

The Sensor Noise Threshold 1 register controls the noise threshold for Capacitive Touch Sensors 1-4.

Bits 7-6 - CS4_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 4.

Bits 5-4 - CS3_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 3.

Bits 3-2 - CS2_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 2.

Bits 1-0 - CS1_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 1.

5.17.2 Sensor Noise Threshold 2 Register

The Sensor Noise Threshold 2 register controls the noise threshold for Capacitive Touch Sensors 5 - 6.

Bits 3-2 - CS6_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 6.

Bits 1-0 - CS5_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 5.

5.18 Standby Channel Register

Table 5.29 Standby Channel Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Standby Channel	-	-	CS6_ STBY	CS5_ STBY	CS4_ STBY	CS3_ STBY	CS2_ STBY	CS1_ STBY	00h

The Standby Channel register controls which (if any) Capacitive Touch Sensors are active during Standby.

Bit 5 - CS6_STBY - Controls whether the CS6 channel is active in Standby.

- '0' (default) - The CS6 channel not be sampled during Standby mode.
- '1' - The CS6 channel will be sampled during Standby Mode. It will use the Standby threshold setting, and the standby averaging and sensitivity settings.

Bit 4 - CS5_STBY - Controls whether the CS5 channel is active in Standby.

Bit 3 - CS4_STBY - Controls whether the CS4 channel is active in Standby.

Bit 2 - CS3_STBY - Controls whether the CS3 channel is active in Standby.

Bit 1 - CS2_STBY - Controls whether the CS2 channel is active in Standby.

Bit 0 - CS1_STBY - Controls whether the CS1 channel is active in Standby.

5.19 Standby Configuration Register

Table 5.30 Standby Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
41h	R/W	Standby Configuration	AVG_ SUM	-	STBY_AVG[2:0]			STBY_ SAMP_ TIME	STBY_CY_TIME [1:0]		1Dh

The Standby Configuration register controls averaging and cycle time for those sensors that are active in Standby.

Bit 7 - AVG_SUM - Determines whether the active sensors will average the programmed number of samples or whether they will accumulate for the programmed number of samples.

- '0' - (default) - The active sensor delta count values will be based on the average of the programmed number of samples when compared against the threshold.
- '1' - The active sensor delta count values will be based on the summation of the programmed number of samples when compared against the threshold.

Bits 5 - 3 - STBY_AVG[2:0] - Determines the number of samples that are taken for all active channels during the sensor cycle as shown in Table 5.31. All samples are taken consecutively on the same channel before the next channel is sampled and the result is averaged over the number of samples measured before updating the measured results.

Table 5.31 STBY_AVG Bit Decode

STBY_AVG[2:0]			NUMBER OF SAMPLES TAKEN PER MEASUREMENT
2	**1**	**0**	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8 (default)
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Bit 2 - STBY SAMP_TIME - Determines the time to take a single sample when the device is in Standby.

- '0' - The sampling time is ~2.56ms.
- '1' (default) - The sampling time is ~1.28ms.

Bits 1 - 0 - STBY_CY_TIME[2:0] - Determines the overall cycle time for all measured channels during normal operation as shown in Table 5.17. All measured channels are sampled at the beginning of the cycle time. If additional time is remaining, then the device is placed into a lower power state for the remaining duration of the cycle.

Table 5.32 STBY_CY_TIME Bit Decode

STBY_CY_TIME[1:0]		OVERALL CYCLE TIME
1	**0**	
0	0	35ms
0	1	70ms (default)
1	0	105ms
1	1	140ms

APPLICATION NOTE: The programmed cycle time is only maintained if the total averaging time for all samples is less than the programmed cycle. The STBY_AVG[2:0] bits will take priority so that if more samples are required than would normally be allowed during the cycle time, the cycle time will be extended as necessary to accommodate the number of samples to be measured.

5.20 Standby Sensitivity Register

Table 5.33 Standby Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
42h	R/W	Standby Sensitivity	-	-	-	-	-	STBY_SENSE[2:0]			02h

The Standby Sensitivity register controls the sensitivity for sensors that are active in Standby.

Bits 2 - 0 - STBY_SENSE[2:0] - Controls the sensitivity for sensors that are active in Standby. The sensitivity settings act to scale the relative delta count value higher or lower based on the system parameters. A setting of 000b is the most sensitive while a setting of 111b is the least sensitive. At the more sensitive settings, touches are detected for a smaller delta C corresponding to a “lighter” touch. These settings are more sensitive to noise however and a noisy environment may flag more false touches than higher sensitivity levels.

APPLICATION NOTE: A value of 128x is the most sensitive setting available. At the most sensitivity settings, the MSB of the Delta Count register represents 64 out of ~25,000 which corresponds to a touch of approximately 0.25% of the base capacitance (or a ΔC of 25fF from a 10pF base capacitance). Conversely a value of 1x is the least sensitive setting available. At these settings, the MSB of the Delta Count register corresponds to a delta count of 8192 counts out of ~25,000 which corresponds to a touch of approximately 33% of the base capacitance (or a ΔC of 3.33pF from a 10pF base capacitance).

Table 5.34 STBY_SENSE Bit Decode

STBY_SENSE[2:0]			SENSITIVITY MULTIPLIER
2	1	0	
0	0	0	128x (most sensitive)
0	0	1	64x
0	1	0	32x (default)
0	1	1	16x
1	0	0	8x
1	0	1	4x
1	1	0	2x
1	1	1	1x - (least sensitive)

5.21 Standby Threshold Register

Table 5.35 Standby Threshold Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
43h	R/W	Standby Threshold	-	64	32	16	8	4	2	1	40h

The Standby Threshold registers stores the delta threshold that is used to determine if a touch has been detected. When a touch occurs, the input signal of the corresponding sensor changes due to the capacitance associated with a touch. If the sensor input change exceeds the threshold settings, then a touch is detected.

5.22 Sensor Base Count Registers

Table 5.36 Sensor Base Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R	Sensor 1 Base Count	128	64	32	16	8	4	2	1	C8h
51h	R	Sensor 2 Base Count	128	64	32	16	8	4	2	1	C8h
52h	R	Sensor 3 Base Count	128	64	32	16	8	4	2	1	C8h
53h	R	Sensor 4 Base Count	128	64	32	16	8	4	2	1	C8h
54h	R	Sensor 5 Base Count	128	64	32	16	8	4	2	1	C8h
55h	R	Sensor 6 Base Count	128	64	32	16	8	4	2	1	C8h

The Sensor Base Count registers store the calibrated “Not Touched” input value from the Capacitive Touch Sensor inputs. These registers are periodically updated by the re-calibration routine.

The routine uses an internal adder to add the current count value for each reading to the sum of the previous readings until sample size has been reached. At this point, the upper 16 bits are taken and used as the Sensor Base Count. The internal adder is then reset and the re-calibration routine continues.

The data presented is determined by the BASE_SHIFT[3:0] bits (see Section 5.5).

APPLICATION NOTE:

5.23 Product ID Register

Table 5.37 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID CAP1006	0	1	0	0	0	1	0	0	44h
		Product ID CAP1005	0	1	0	0	0	1	0	1	45h

The Product ID register stores a unique 8-bit value that identifies the device.

5.24 Manufacturer ID Register

Table 5.38 Vendor ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Vendor ID register stores an 8-bit value that represents SMSC.

5.25 Revision Register

Table 5.39 Revision Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	1	0	0	0	0	0	0	1	81h

The Revision register stores an 8-bit value that represents the part revision.

Chapter 6 Package Information

6.1 CAP1006 and CAP1005 Package Drawings

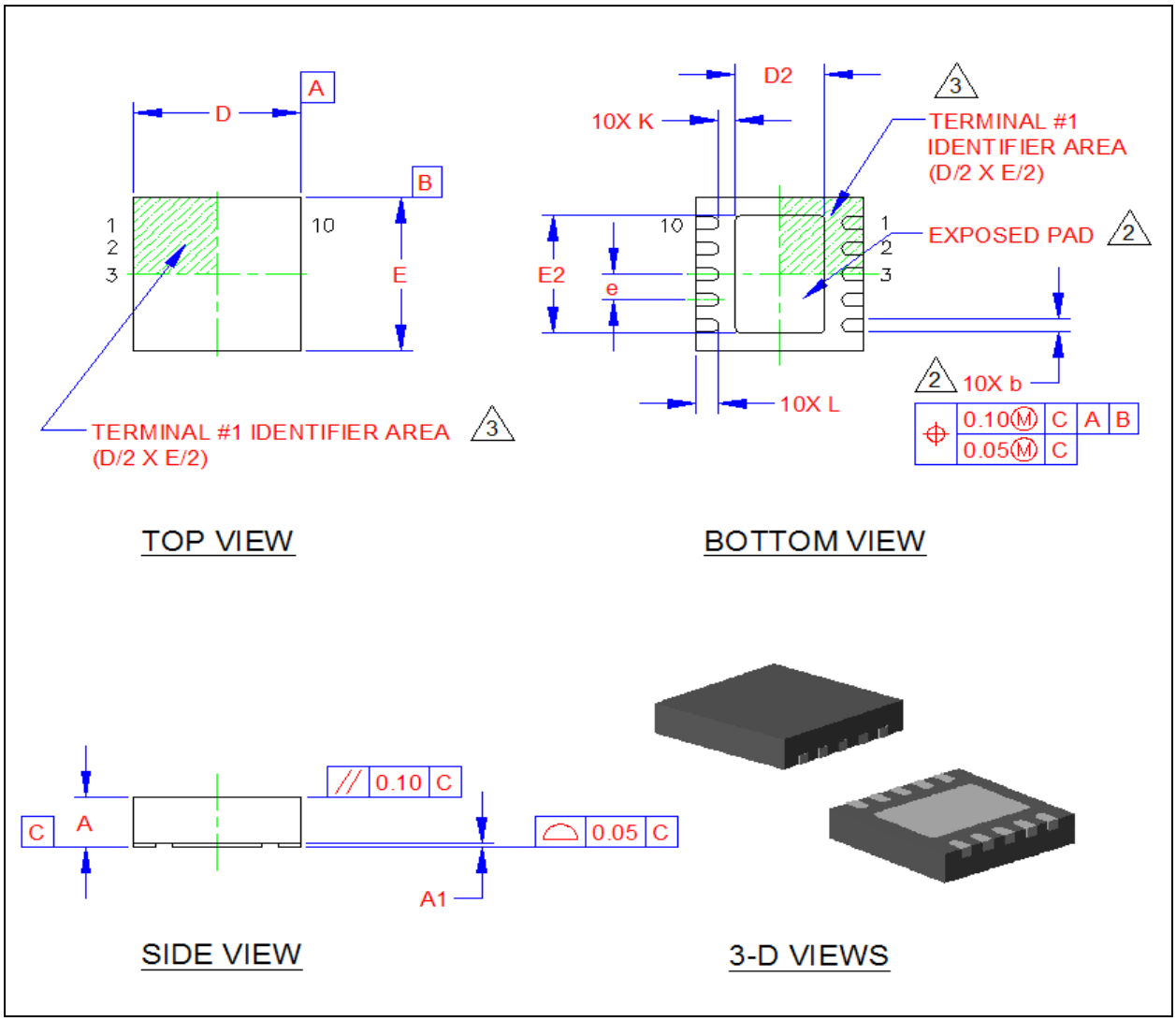


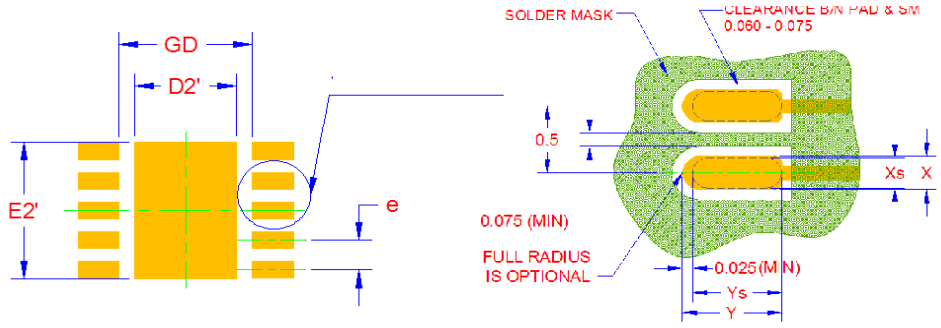
Figure 6.1 10-Pin DFN 3mm x 3mm Package Drawing

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D2	1.50	1.60	1.70	2	X EXPOSED PAD SIZE
E2	2.20	2.30	2.40	2	Y EXPOSED PAD SIZE
L	0.35	0.40	0.45	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD, AS WELL AS THE TERMINALS. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.2 10-Pin DFN 3mm x 3mm Package Dimensions



PCB LAND PATTERN

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD	2.10	-	2.20
D2'	-	1.60	1.60
E2'	-	2.30	-
Pad: X	-	0.28	0.28
Pad: Y	-	0.69	0.69
e		0.50	

Figure 6.3 10-Pin DFN 3mm x 3mm PCB Footprint

6.2 Package Marking

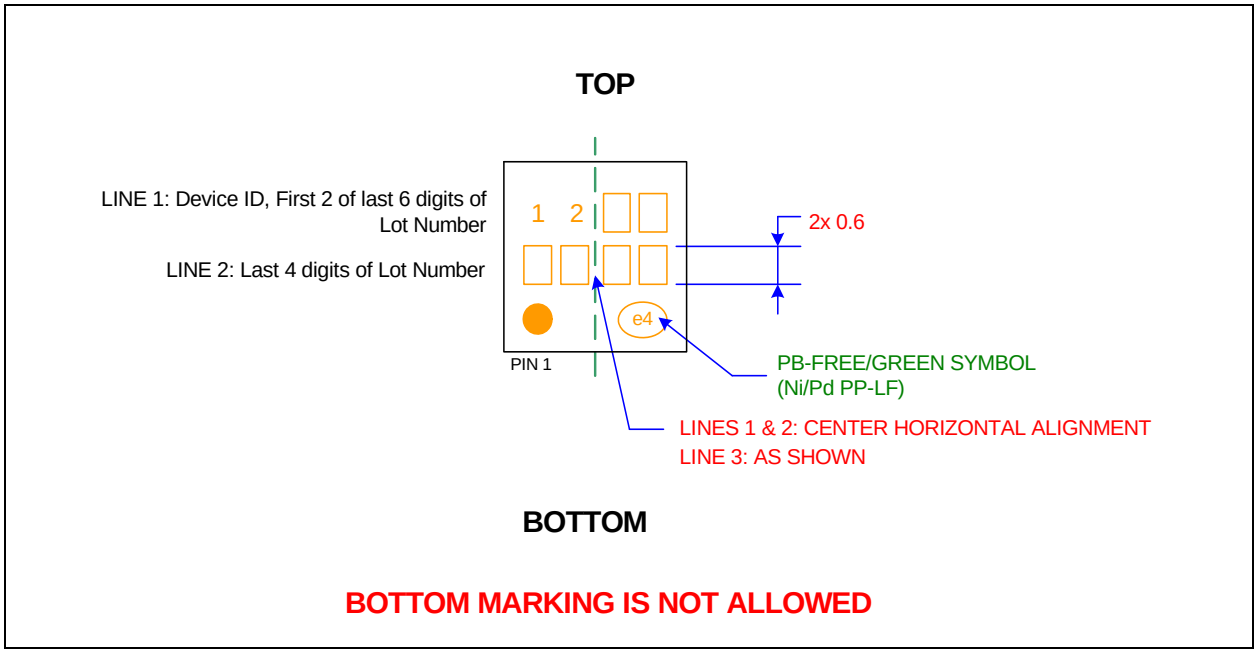


Figure 6.4 CAP1006-1 Package Markings

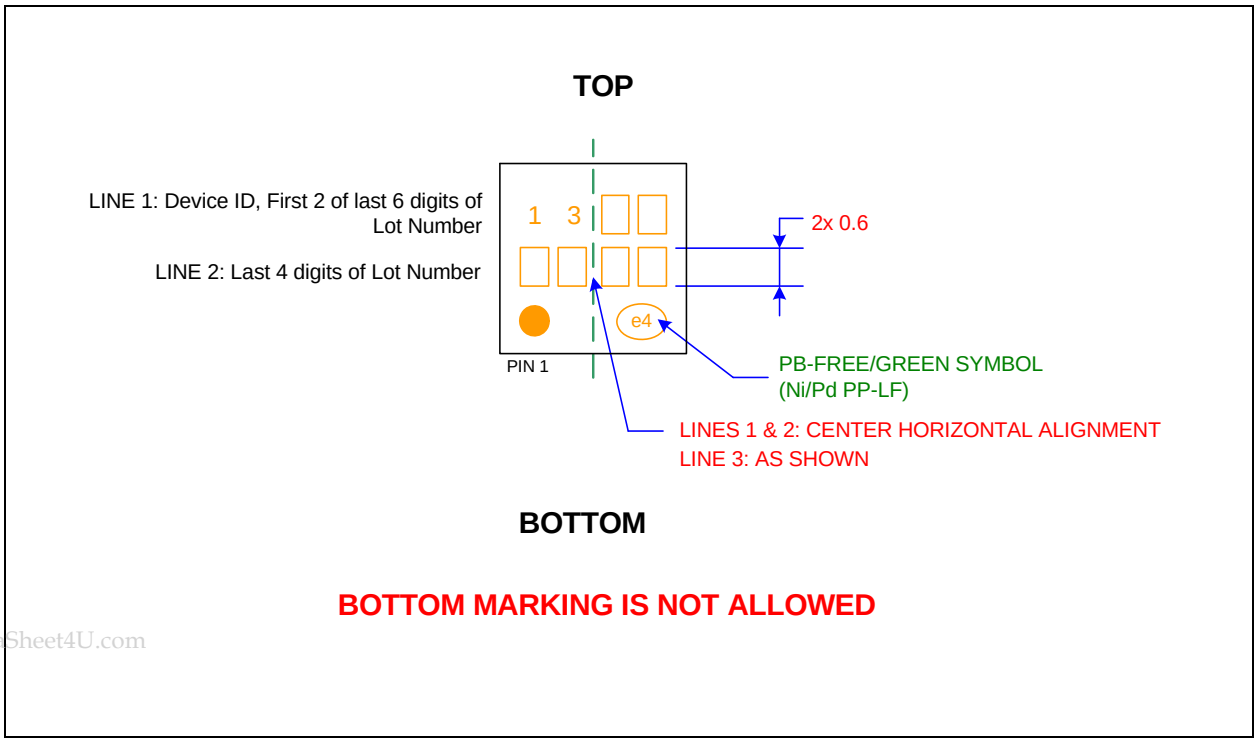


Figure 6.5 CAP1006-2 Package Markings

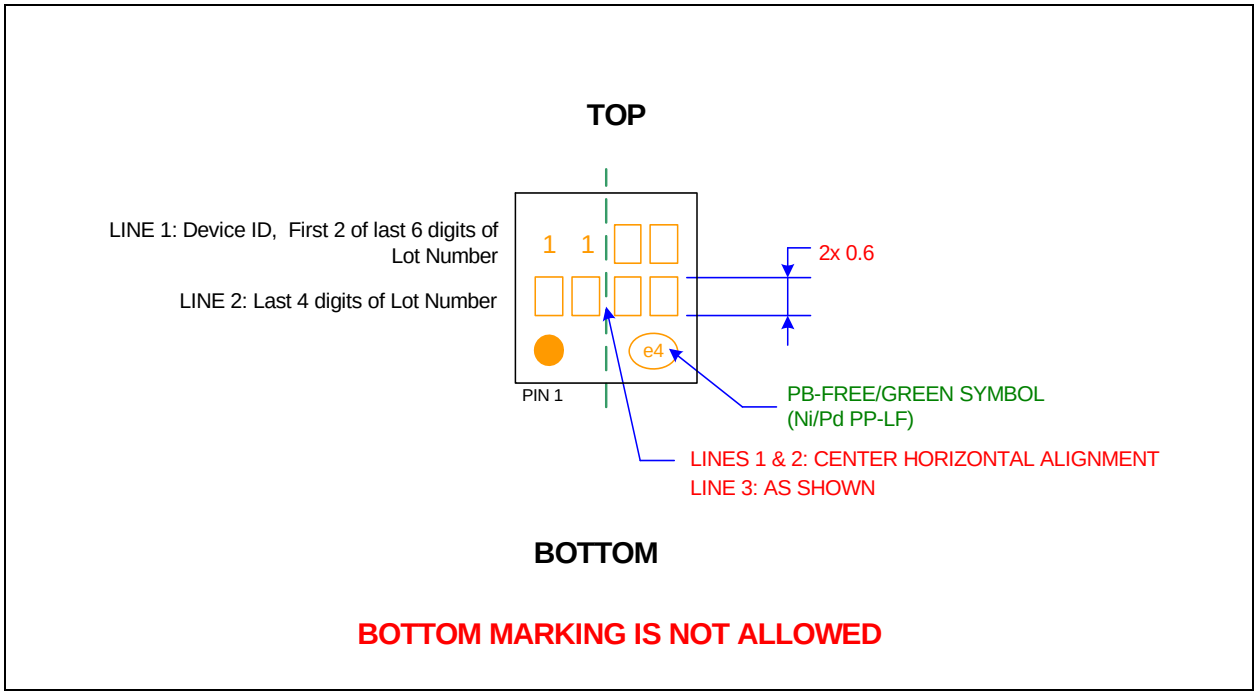


Figure 6.6 CAP1005 Package Markings

Chapter 7 Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (08-05-09)	Features	“TBD” replaced with “3uA” under Low Power Operation
	General Description	Deep sleep drawing “5uA” of current changed to “3uA”
	Table 2.2, "Electrical Specifications"	Table updated: - Current Measurement, ISTBY - changed the typical column to 160, max to 210. Changed the conditions to read: " Standby state active, one sensor monitored, default conditions (8 avg, 70ms cycle time)" - Current Measurement, IDSLEEP -changed the TYP column value to 3 and max to 10.
	Section 3.1.1, "SMBus (I2C) Communications"	The following text deleted: “The SPI_CS# pin is not used and any data presented to this pin will be ignored.”
	Section 6.2, "Package Marking"	Updated package markings per new standards
Rev. 1.0 (06-16-09)	Document title modified; reel size added to ordering information; updates to pinout, general description and register set. “System RESET pin” removed from features	
	Chapter 1, Pin Description	Pin tables modified adding SPI to “ALERT# / BC_IRQ#” pin
	Table 2.1, "Absolute Maximum Ratings"	Notes following table modified
	Figure 3.1, "SPI Timing"	Updated figure
	Section 3.6, "BC-Link Interface (CAP1006-2 only)"	Removed “8051” from 2nd paragraph
	Chapter 4, General Description	Second to last paragraph removed, not needed as clarification follows
	Section 4.1, "Power States"	Removed mention of LED driver outputs
	Table 5.1, "Register Set in Hexadecimal Order"	Updated text and register descriptions for incorrect #’s Cap Sense channels
	Section 6.2, "Package Marking"	Updated package markings
Rev. 0.56 (5/1/09)	General	Fixed typos and updated text as necessary. Cleaned up system diagrams
	Section 5.5, "Sensitivity Control Register"	Renamed bit fields

Table 7.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
	Section 5.6, "Configuration Register"	Renamed bits 5 and 6
Rev. 0.53 (4/23/09)	Section 3.4, "SPI Interface (CAP1005 only)"	Updated section to describe Normal operation
Rev. 0.52 (4/17/09)	General	Initial document creation